

Efficient Matrix Multiplications on RISC-V MCUs

$$\begin{pmatrix} 0 & 1 & 0 & \dots & 0 \\ 1 & 0 & 1 & \dots & 1 \\ 0 & 0 & 1 & \dots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 1 & 0 & \dots & 1 \end{pmatrix}$$

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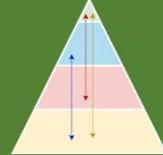
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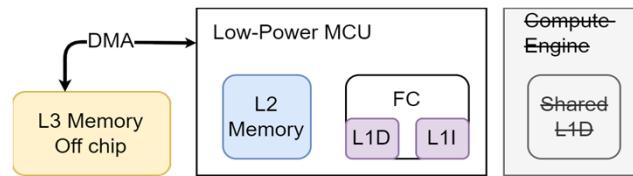
- > GAP8
- > Leverage Dot product vector instructions
- > New Multi-level memory hierarchy
- > Approximate Computing
- > Modified BLIS (BLAS-like Library Instantiation Software)



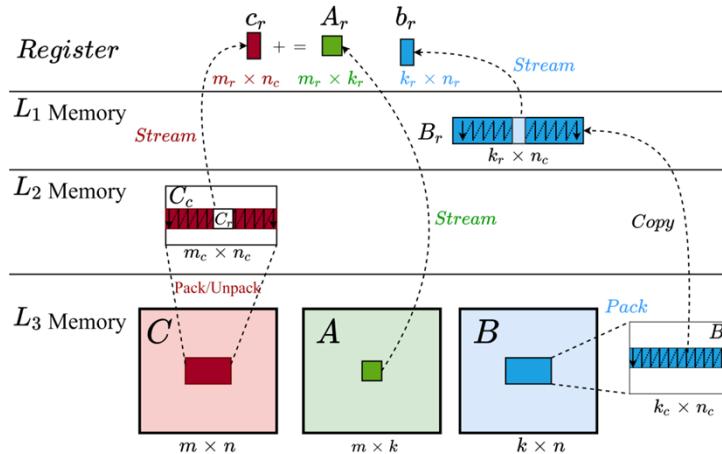
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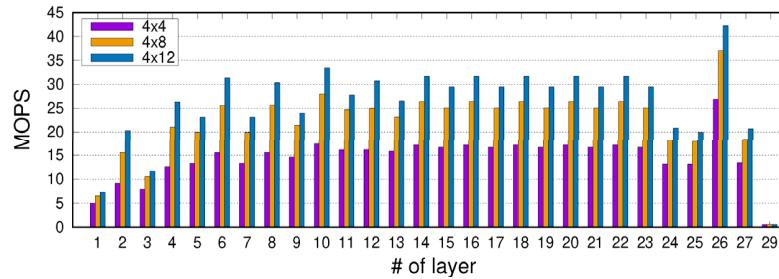
GAP8 Memory Architecture



Matrix Packing, Copying, Streaming



Performance on Different Dimension of Microkernel and Convolutional Layers of MobileNet V1



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Proposed GEMM algorithm (B3C2Ao)

```

L1   for ( j_c = 0; j_c < n; j_c += n_c ) {
L2     for ( p_c = 0; p_c < k; p_c += k_c ) {
L3       B_c <- B(p_c : p_c + k_c - 1, j_c : j_c + n_c - 1); // Pack
L4       for ( i_c = 0; i_c < m; i_c += m_c ) {
L5         C_c <- C(i_c : i_c + m_c - 1, j_c : j_c + n_c - 1); // Pack
L6         for ( p_r = 0; p_r < k_c; p_r += k_r ) {
L7           for ( i_r = 0; i_r < m_c; i_r += m_r ) {
L8             for ( j_r = 0; j_r < n_c; j_r += 1 ) // Micro-kernel
L9               C_c(i_r : i_r + m_r - 1, j_r)
L10              += A_c(i_r : i_r + m_r - 1, p_r : p_r + k_r - 1)
L11              * B_c(p_r : p_r + k_r - 1, j_r);
L12           }
L13         }
L14       }
L15     }
L16   }
L17   C(i_c : i_c + m_c - 1, j_c : j_c + n_c - 1) <- C_c; // Unpack
    } }
```

Proposed micro-Kernel (Loop 6)

```

gemm_ukernel_Aresident_gap8( int nc, signed char *A, int lda,
                           signed char Br , signed char Cc )
{
    int jr, baseCB = 0;
    v4s A0, A1, A2, A3, // Columns of the 4x4 micro-tile Ar
    br, cr; // Columns of Br, Cr

    // Load the columns of the 4x4 micro-tile Ar into vector
    // registers
    // Simulated in software using the v4s datatype
    A0 = ((v4s) (&A[0])); A1 = ((v4s) (&A[1*lda]));
    A2 = ((v4s) (&A[2*lda])); A3 = ((v4s) (&A[3*lda]));

    // Transposition of Ar omitted for brevity
    // ...
    for ( jr = 0; jr < nc; jr++ ) { // Loop 6
        // Load the jr-th columns of Cr, Br into two vector registers
        cr = ((v4s) (&Cr[baseCB]));
        br = ((v4s) (&Br[baseCB]));

        // Update i-th entry of cr as cr[i] += Ai * br, i=0,1,2,3,
        // The GAP8 dot product is realized in software via the
        // gap8_dotp4 instruction
        cr[0] += gap8_dotp4(A0, br); cr[1] += gap8_dotp4(A1, br);
        cr[2] += gap8_dotp4(A2, br); cr[3] += gap8_dotp4(A3, br);

        // Store the column of Cr in memory. No vector support in
        GAP8
        Cr[baseCB+0] = cr[0]; Cr[baseCB+1] = cr[1];
        Cr[baseCB+2] = cr[2]; Cr[baseCB+3] = cr[3];

        baseCB += 4; // Prepare for next iteration
    }
}
```

Runtimes on Different micro-kernel dimensions

